

Notice of Allowability	Application No.	Applicant(s)
	10/810,307	LAUER ET AL.
	Examiner Jaison Joseph	Art Unit 2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTO-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. This communication is responsive to amendment filed on 08/01/2007.
2. The allowed claim(s) is/are 1 – 10, 12, 13, and 17 – 20 renumbered as 1 - 16 respectively.
3. Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All
 - b) Some*
 - c) None
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) hereto or 2) to Paper No./Mail Date _____.
 - (b) including changes required by the attached Examiner's Amendment /Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

<ol style="list-style-type: none"> 1. <input type="checkbox"/> Notice of References Cited (PTO-892) 2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) 3. <input type="checkbox"/> Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____ 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit of Biological Material 	<ol style="list-style-type: none"> 5. <input type="checkbox"/> Notice of Informal Patent Application 6. <input checked="" type="checkbox"/> Interview Summary (PTO-413), Paper No./Mail Date _____ 7. <input checked="" type="checkbox"/> Examiner's Amendment/Comment 8. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance 9. <input type="checkbox"/> Other _____
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EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Michael R. Cannatti on 09/28/2007.

The application has been amended as follows:

Specification:

Please amend paragraph 052 as follows:

[052] As will be appreciated, the present invention may be implemented in a computer accessible medium including one or more data structures representative of the circuitry included in the system described herein. Generally speaking, a computer accessible medium may include storage media such as magnetic or optical media, e.g., disk, CD-ROM, or DVD-ROM, volatile or non-volatile memory media such as RAM (e.g., SDRAM, RDRAM, SRAM, etc.), ROM, PROM, EPROM, EEPROM, etc., as well as media accessible via transmission media or signals such as electrical, electromagnetic, or digital signals, conveyed via a communication medium such as a network and/or a wireless link. For example, data structure(s) of the circuitry on the computer accessible medium may be read by a program and used, directly or indirectly, to implement the hardware comprising the circuitry described herein. For example, the data structure(s) may include one or more behavioral-level descriptions or register-transfer level (RTL)

descriptions of the hardware functionality in a high level design language (HDL) such as Verilog or VHDL. The description(s) may be read by a synthesis tool which may synthesize the description to produce one or more netlist(s) comprising lists of gates from a synthesis library. The netlist(s) comprise a set of gates which also represent the functionality of the hardware comprising the circuitry. The netlist(s) may then be placed and routed to produce one or more data set(s) describing geometric shapes to be applied to masks. The masks may then be used in various semiconductor fabrication steps to produce a semiconductor circuit or circuits corresponding to the circuitry. Alternatively, the data structure(s) on computer accessible medium may be the netlist(s) (with or without the synthesis library) or the data set(s), as desired. In yet another alternative, the data structures may comprise the output of a schematic program, or netlist(s) or data set(s) derived therefrom. While a computer accessible medium may include a representation of the present invention, other embodiments may include a representation of any portion of the decoding and demapping system and circuitry (e.g., log2x, module, antilog module, adders, subtractors, etc.).

Claims:

Claim 5 rewrite as: The method of claim 1, wherein the processing of the gain value and noise value to determine a branch metric further comprises using a [

processor to calculate a branch metric (M) using the equation $M = \left[\frac{1|H|^2 k_{loc}^2}{C_1 \sigma^2} - C_2 \right]$

, where H is the scalar Rain value, C₁ is the first constant for a transmit constellation, C₂

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s the second constant for a the transmit constellation, k_{loc} is a location information scaling factor and σ^2 is the noise value.

Claim 12 rewrite as: An article of manufacture having at least one recordable medium having stored thereon executable instructions and data which, when executed by at least one processing device, cause the at least one processing device to compute a branch metric for a Viterbi decoder, comprising implementing a multiplication operation of a first term and a second term in the branch metric computation by:

adding a log of the first term to a log of the second term to form a first sum; and determining the antilog of the first sum, wherein the processing device computes a branch metric for a Viterbi decoder by

computing a $\log_2 |H|^2$ value, where H represents a scalar gain value for a transmission channel;

subtracting a $\log_2 \sigma^2$ value from the $\log_2 |H|^2$ value to form a first sum, where σ^2 represents a noise variance value for the transmission channel;

subtracting a $\log_2 C_1$ value from the first sum to form a second sum, where the C_1 value has been pre-computed and stored in memory;

computing an antilog of the second sum; and

subtracting a C_2 value which has been stored in memory from the antilog of the second sum to form a the branch metric.

Claim 17 rewrite as: An apparatus for decoding a signal, the apparatus comprising:

means for receiving a sampled signal;

means for demapping the received sampled signal into a branch metric comprising means for performing multiplication operations in a log domain using an adder circuit and means for performing division operations in a log domain using an subtractor circuit; and means for providing the branch metric a Viterbi decoder, where the means for demapping comprises a means for calculating a branch metric (M) using the equation $M = \left[\frac{1|H|^2 k_{loc}^2}{C_1 \sigma^2} - C_2 \right]$ where H represents a scalar gain value for a transmission channel, C₁ is a first pre-computed constant for a transmit constellation, C₂ is a second pre-computed constant for a the transmit constellation, k_{loc} is a location information scaling factor, and σ² represents a noise variance value for the transmission channel.

Claim 18 rewrite as: The apparatus of claim 17 An apparatus for decoding a signal, the apparatus comprising:

means for receiving a sampled signal;
means for demapping the received sampled signal into a branch metric
comprising means for performing multiplication operations in a log domain
using an adder circuit and means for performing division operations in a
log domain using an subtractor circuit; and
means for providing the branch metric a Viterbi decoder, where the means for

demapping comprises a means for calculating a branch metric (M) using 1

the equation $M = \left[\frac{1|H|^2}{C_1\sigma^2} - C_2 \right]$ where H represents a scalar gain value for a

transmission channel, C_1 is a first pre-computed constant for a transmit constellation, C_2 is a second pre-computed constant for a the transmit constellation, k_{loc} is a location information scaling factor, and σ^2 represents a noise variance value for the transmission channel.

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance: Claims 1 – 10, 12, 13, 17 – 20 are allowable over prior art of record. The prior art of record failed to teach In an integrated circuit wireless communication device, a method for Viterbi decoding comprising: receiving a transmitted signal over a channel substantially characterized by a scalar gain value and a noise value; processing the gain value and noise value to determine a branch metric by determining a log of the scalar gain value and subtracting therefrom a log of the noise value and subtracting therefrom the log of a first constant to form a first sum, and determining an antilog of the first sum and subtracting therefrom a second constant to form a second sum, the second sum corresponding to the branch metric; and providing the branch metric to a Viterbi decoder as claimed in independent claim 1 and similarly claimed in independent claim 12, 17, and 18. thus claims 1 – 10, 12, 13, 17 – 20 are novel an unobvious over prior art of record.

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Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

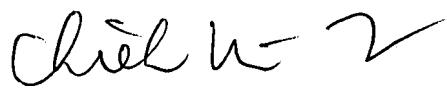
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jaison Joseph whose telephone number is (571) 272-6041. The examiner can normally be reached on M-F 9:30 - 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jaison Joseph
09/28/2007


CHIEH M. FAN
SUPERVISORY PATENT EXAMINER